UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,699	11/18/2003	Scott Alan Geye	MV03-010	5395

7590 05/19/2010

Michael B. Atlass
Unisys Corporation
Unisys Way, MS/E8-114
Blue Bell, PA 19424-0001

EXAMINER	
ZHE, MENG YAO	
ART UNIT	PAPER NUMBER
2195	

MAIL DATE	DELIVERY MODE
05/19/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,699	GEYE ET AL.	
	Examiner	Art Unit	
	MENGYAO ZHE	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 13, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Jaiswal et al., Pub No. 2005/0044127 (hereafter Jaiswal).

4. Jaiswal was cited in the previous office action.

5. As per claims 1, 13, 25 Jaiswal teaches the invention as claimed including a method of associating a processor with a set of computer-readable instructions in a multiprocessor system, comprising:

selecting a first cluster from at least two clusters (Para 38: the domain with multiple entities corresponds to a cluster), each cluster having an associated priority indicator, where the selected cluster is selected as a function of its priority indicator (Para 38: the load factor of an entire domain corresponds to the priority indicator);

selecting a first processor from the cluster, the cluster comprising at least one other processor, each processor having an associated priority indicator, where the selected first processor is selected as a function of its priority indicator (Para 24, 25, 60);

associating the first processor with a first set of computer-readable instructions (Para 60: the whole point of the Jaiswal's invention to associate a relatively less loaded server or processor to process an incoming request or packet);

causing the first processor to execute the first set of computer-readable instructions (Para 18, 27).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al., Patent No. 6,105,053 (hereafter Kimmel) in view of Kaushik et al., Patent No. 7,191,349 (hereafter Kaushik).

8. Kimmel and Kaushik were cited in the previous office action.

9. As per claims 1, 13, Kimmel teaches the invention as claimed including a method of associating a processor with a set of computer-readable instructions in a multiprocessor system, comprising:

selecting a first cluster from at least two clusters (Fig 1A: all JP that routes to the same shared memory corresponds to a cluster. For example, JP0 and JP1 make up one cluster.), each cluster having an associated priority indicator, where the selected cluster is selected as a function of its priority indicator (Col 9, lines 28-38: each node on level 1, which corresponds to a cluster, gets its own run queue. Col 6, lines 10-15, 54-61: each thread group has its own priorities. Each queue in all of the node levels contains the thread groups and their associated priorities. Thus each node on level 1 will have priority values associated with it. Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47: load value for each node can be measure using priorities found in its queues, which can then be used by the scheduler perform load balancing among any nodes at any level, thus selecting a node to execute a thread group when other nodes are overloaded);

selecting a first processor from the cluster, the cluster comprising at least one other processor (Fig 1B, node 110 corresponds to a cluster, unit 100 and 101 are processors.), each processor having an associated priority indicator, where the selected first processor is selected as a function of its priority indicator (Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47);

associating the first processor with the first set of computer-readable instructions (Col 13, line 40-Col 14, line 27) and causing the first processor to execute the first set of computer-readable instructions (Column 6, lines 15-21).

Kimmel teaches selecting a cluster and a processor from a cluster based on its load, which is a function of the priority of threads running on the cluster and the processors within the cluster (Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47). Kimmel does not specifically teach that the cluster and the processor having their own priority value, which directly indicates the priority of the cluster or processor.

However, Kaushik teaches a processor have a priority indicator directly indicating the priority of the processor. Furthermore, the priority of the processor is the function of the priorities of tasks that runs on the processor for the purpose of letting the priority of tasks running on the processor to represent the priority of the processor itself (Column 3, lines 13-25).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Kimmel where cluster or processor are chosen based on its load value that is the function of priorities of their running tasks, with the cluster or processor having its own priority value that directly indicates the priority of the cluster or processor, as taught by Kaushik, because it allows the priority of tasks that are running on the processor to directly represent the priority of the processor itself.

10. As per claims 2, 14, Kimmel teaches wherein the processors comprise CPUs (Fig 1A; Col 5, lines 15-21).

11. As per claims 3, 15, Kimmel teaches wherein the first set of computer-readable instructions comprise an application program (Col 5, line 60 to Col 6, line 5: computer-readable instructions are application programs).

12. As per claims 4, 16, Kimmel teaches wherein the first set of computer-readable instructions comprise an processing thread (Col 5, line 60 to Col 6, line 5).

13. As per claims 5, 17, Kimmel teaches wherein the priority indicator associated with each processor is a function of the priority of each selected set of computer-readable instructions associated with the processor (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47).

14. As per claims 6, 18, Kimmel teaches wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47: the load of the level 1 nodes are based on the sub-tree beneath it. Since the

processors are level 0, below level 1 of the clusters, priority of level 1 is a function of priority of level 0).

15. As per claims 7, 19, Kimmel teaches wherein the priority indicator for each cluster is a function of the priority of each processor in the cluster (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27).

16. As per claims 8, 20, Kimmel teaches the step of adjusting the priority of the selected processor based on the priority of the first set of computer-readable instructions (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27).

17. As per claims 9, 21 Kimmel teaches the steps of selecting a second set of computer readable instructions and repeating the acts of selecting a cluster and selecting a processor; and associating the selected processor with the second set of computer-readable instructions. (Col 11, lines 13-22; Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27: clearly, the invention as disclosed by Kimmel may be repeated on all threads that need to be executed.)

18. As per claims 10, 22, Kimmel teaches executing the first set of computer-readable instructions on the associated processor (Col 9, lines 28-38; Col 6, lines 10-15, 54-61; Col 13, line 40-Col 14, line 27).

19. As per claims 11, 23, Kimmel teaches wherein a cluster other than the first cluster is selected if the other cluster has a processor associated with the first set of computer readable instructions and the other cluster has no processors associated with the first set of computer-readable instructions (Col 1, lines 59-67; Col 12, lines 35-55: the entire purpose of Kimmel's invention is to improve infinity, which means selecting a processor to run a thread in a thread group if it is already running other threads in the same thread group. Processors are grouped under different nodes or clusters).

20. As per claims 12, 24, Kimmel teaches wherein a processor other than the first processor is selected if the first processor has already been associated with the first set of computer-readable instructions and the other processor has no association with the first set of computer-readable instructions (Col 1, lines 59-67; Col 12, lines 35-55).

21. As per claim 25, it teaches all of claim 1 in addition to where the priority is a function of the priority of the set of computer readable instructions, which is also taught by Kaushik in Column 3, lines 15-25.

22. As per claims 26-36, they are system claims of claims 1-12. Therefore, they are rejected as claims 2-12 above.

Response to Arguments

23. Applicant's arguments filed on 3/1/2010 have been fully considered but are not persuasive.

24. In the remark, the applicant argued that:

i) The underlying architecture employed in Jaiswal renders it inapplicable to a multiprocessor system as recited in Applicant's claims because the sender has knowledge of the recipients before the session is initiated whereas the applicant's invention does not have this knowledge.

ii) There are no instructions to be executed at each processor.

iii) The combination of Kaushik and Kimmel is purely based on hindsight.

25. The Examiner respectfully disagrees, as to point:

i) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e. that the system has no knowledge of the recipient before taking action) are not recited in the rejected claim(s). Although the claims are interpreted in

light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant merely claimed for a multiprocessor system without claiming its underlying architecture, and Jaiswal does teach a multiprocessor system as shown in Fig 1.

Furthermore, the applicant argues that the processor that is suppose to receive the instruction is not known in advance where as in Jaiswal's invention, whoever that gets the instruction/task IS known in advance. The applicant seems to argue that Jaiswal could NOT possibly teach selecting who is supposed to execute the instructions since the receiving node is already known in advance. In other words, one would not be selecting A to do a job if A has already been designated to do the job from the get go.

In response to this, the Examiner points out that one of the things that Jaiswal selects who is supposed to execute the instructions are not necessarily the ultimate receiving entity, but the intermediate nodes that is needed for relaying and processing. For example, in a system where A is transmitting to B, it will have to go through either R1 or R2. Jaiswal is selecting whether R1 or R2 will perform the relaying job based on the load of R1 and R2 (Para 29-30).

ii) Jaiswal teaches instructions to be executed at each node, including protocols—a set of instructions--used for communication (Para 18, 27: functions/calls/protocol all include executable instructions). Whatever is being

performed at each node corresponds to the instruction that is to be executed at each selected node.

iii) In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

More specifically, it is not a logical leap to conclude that because clusters are the sum of processors, it would have been obvious to one of ordinary skill in the art to deduce that the priorities of a cluster is a function of priorities of threads in the cluster as it is analogous to the idea that the characteristic of individual elements contributes to the characteristic of the entire group of elements. Here, the characteristic corresponds to the priority.

The applicant also argues that the claimed invention does not require that the cluster priority be a function of the priority of the processors while the Examiner has specifically interpreted the claim to be so. However, because the claim is broad in the sense that it only claims that there is a priority associated with the cluster and does not say how this priority value was calculated, the Examiner merely found an example of a cluster having a priority value, which in

this case happens to be a priority value that is the function of its subcomponents. Of course, if the applicant specifically claims that the cluster priority value is not a function of its subcomponents, the current prior art would no longer read on it. But since the claim is not this specific, the current art reads on the current claim.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/

Supervisory Patent Examiner, Art Unit 2195

/Mengyao Zhe/